



Microprocessor Architectures and Systems: RISC, CISC and DSP

Steve Heath

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Microprocessor Architectures and Systems: RISC, CISC, and DSP focuses on the developments of Motorola's CISC, RISC, and DSP processors and the advancements of the design, functions, and architecture of microprocessors.

The publication first ponders on complex instruction set computers and 32-bit CISC processors. Discussions focus on MC68881 and MC68882 floating point coprocessors, debugging support, MC68020 32-bit performance standard, bus interfaces, MC68010 SUPERVISOR resource, and high-level language support. The manuscript then covers the RISC challenge, digital signal processing, and memory management and caches. Topics include implementing memory systems, multitasking and user/supervisor conflicts, partitioning the system, cache size and organization, DSP56000 family, MC88100 programming model, M88000 family, and the 80/20 rule.

The text examines the selection of a microprocessor architecture, changing design cycle, semiconductor technology, multiprocessing, and real-time software, interrupts, and exceptions. Concerns include locating associated tasks, MC88100 interrupt service routines, single- and multiple-threaded operating systems, and the MC68300 family.

The publication is a valuable reference for computer engineers and researchers interested in microprocessor architectures and systems.

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